REMARKS

The Examiner has rejected Claims 1-9 under 35 U.S.C. 102(e) as being anticipated by Lee et al. (U.S. Patent No. 2003/0009599). Applicant respectfully disagrees with such rejection, especially in view of the amendments made hereinabove to independent Claim 1. Specifically, applicant has amended independent Claim 1 to at least substantially include the subject matter of independent Claim 8.

With respect to the subject matter of independent Claim 8 (now at least substantially incorporated into independent Claim 1), the Examiner has relied on Figures 2 and 3, in addition to the following excerpt from Lee to make a prior art showing of applicant's claimed "storing statistics associated with a communication of data through at least one module in a switch" (as amended-see this or similar, but not necessarily identical language in the independent claims).

> "MAC 220 helps to transfer incoming data from PHY 216 to memory logic 222 and outgoing data from memory logic 222 to PHY 218. MAC 220 also transfers incoming data from PHY 216 to memory logic 224 that includes a lookup engine 226 and a lookup memory 228. In a specific implementation, the lookup engine distinguishes among different classes or types of data traffic and uses the lookup memory to determine how to treat data traffic based on its class or type. The lookup memory may hold one or more tables of data that supplies guidance for directing or otherwise treating the data traffic." (Paragraph 0025 - emphasis added)

Applicant respectfully asserts that Figures 2 and 3 from Lee only generally show RPR network cards 200, 300, and 302, where the card 200 generally illustrates memory logic 224 that includes a lookup engine 226 and a lookup memory 228. Furthermore, the excerpt relied upon by the Examiner merely teaches that "the lookup engine distinguishes among different classes or types of data traffic and uses the lookup memory to determine how to treat data traffic based on its class or type" and that "[t]he lookup memory may hold one or more tables of data that supplies guidance for directing or otherwise treating the data traffic" (emphasis added).

However, the Figures and the excerpt fail to teach "storing statistics associated with the communication of data through at least one module in the switch" (emphasis added), as claimed by applicant. Clearly, disclosing "tables of data that supplies guidance for directing or otherwise treating the data traffic" (emphasis added), as in Lee, fails to teach "storing statistics associated with a communication of data" (emphasis added), as claimed by applicant.

Additionally, with respect to the subject matter of independent Claim 8 (at least substantially incorporated into independent Claim 1), the Examiner has relied on items 204, 206, 214, and 222 of Figure 2, in addition to Paragraph 0025 from Lee to make a prior art showing of applicant's claimed "evaluating the statistics to generate a link signal representative of desired links/ports to be aggregated" (as amended - see this or similar, but not necessarily identical language in the independent claims).

Applicant respectfully asserts that Figure 2 from Lee generally illustrates a working channel 204, a protection channel 206, fault handling logic 214, and memory logic 222, where "[f]ault handling logic 214 responds to fault indications from memory logic 222, and, under certain circumstances..., can reconfigure memory logic 222 and priority filter 238 to cause card 200 to form a bridge redirecting data between working channel 204 and protection channel 206" (Paragraph 0028 - emphasis added).

However, disclosing fault handling logic 214 for responding to fault indications, as in Lee, fails to even suggest "evaluating the statistics" (emphasis added), as claimed by applicant. Furthermore, reconfiguring memory logic 222 and priority filter 238 to cause the card 200 to form a bridge redirecting data between channels, as in Lee, in no way suggests "evaluating the statistics to generate a link signal representative of desired links/ports to be aggregated" (emphasis added), as claimed by applicants.

In addition, applicant respectfully asserts that Paragraph 0025 from Lee merely teaches that "the lookup engine distinguishes among different classes or types of data traffic and uses the lookup memory to determine how to treat data traffic based on its

class or type" and that "[t]he lookup memory may hold one or more tables of data that supplies guidance for directing or otherwise treating the data traffic" (emphasis added). However, disclosing "tables of data that supplies guidance for directing or otherwise treating the data traffic" (emphasis added), as in Lee, fails to teach or even suggest "evaluating the statistics to generate a link signal representative of desired links/ports to be aggregated" (emphasis added), as claimed by applicant.

Still yet, with respect to the subject matter of independent Claim 8 (at least substantially incorporated into independent Claim 1),, the Examiner has relied on items 208, 210, and 214 of Figure 2; and items 326, 332, 336, and 338 of Figure 3 from Lee to make a prior art showing of applicant's claimed "selectively activating a link aggregation port to respond to the link signal and to dynamically set one or more switch modules' external terminals to selectively aggregate information to and from the switch modules" (see this or similar, but not necessarily identical language in the independent claims).

Applicant respectfully asserts that Figure 3 from Lee only generally illustrates a working channel output 326, a fault indication ("UFI") signal detector 332, a protection channel input 336, and a protection channel output 338. Further, in Paragraph 0036, Lee teaches that "[u]nder certain circumstances..., one or both of filters 301, 303.... and consequently one or both of respective cards 300, 302, may be placed in bridge mode" and that "[i]n the case of filter 301, bridge mode causes all of data Wy, Py, Wa, and Pa to be passed from logic 328 to output 338." Further, Paragraph 0036 in Lee teaches that "[i]n the case of filter 303, bridge mode causes all of data Wy, Py, Wa, and Pa to be passed from logic 328 to output 326" and "in at least some cases, bridge mode can be adopted by one or more of cards 300, 302 to respond to an event such as a disruption in a way that is transparent and nonintrusive to logic 328 and to a system that communicates with the working and protective channels via logic 328."

However, merely disclosing different filters where data is passed to different outputs, fails to even suggest "selectively activating a link aggregation port to respond to the link signal and to dynamically set one or more switch modules' external terminals to

selectively aggregate information to and from the switch modules" (emphasis added), as claimed by applicant.

Further, applicant respectfully asserts that Figure 2 from Lee only generally illustrates low voltage differential signal ("LVDS") connections 208, 210 and fault handling logic 214, where "[the] input and output low voltage differential signal ("LVDS") connections 208, 210...may be routed to a companion card for use in packet circuit emulation ("PACE") technology" (Paragraph 0023), and the "[f]ault handling logic 214 responds to fault indications from memory logic 222" (Paragraph 0028).

However, generally disclosing LVDS connections which may be routed to a companion card for use in PACE technology, in conjunction with fault handling logic for responding to fault indications, as in Lee, in no way suggests "selectively activating a link aggregation port to respond to the link signal and to dynamically set one or more switch modules' external terminals to selectively aggregate information to and from the switch modules" (emphasis added), as claimed by applicant. Clearly, generally disclosing fault handling logic in no way suggests "selectively aggregat[ing] information to and from the switch modules" (emphasis added), as claimed by applicant.

The Examiner is reminded that a claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described in a single prior art reference. *Verdegaal Bros. v. Union Oil Co. Of California*, 814 F.2d 628, 631, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987). Moreover, the identical invention must be shown in as complete detail as contained in the claim. *Richardson v. Suzuki Motor Co.*868 F.2d 1226, 1236, 9USPQ2d 1913, 1920 (Fed. Cir. 1989). The elements must be arranged as required by the claim.

This criterion has simply not been met by the above reference, as noted above. Thus, a notice of allowance or specific prior art showing of each of the foregoing claim elements, in combination with the remaining claimed features, is respectfully requested.

Applicant further notes that the prior art is also deficient with respect to the dependent claims. For example, with respect to Claim 7, the Examiner has relied on Figure 2 from Lee to make a prior art showing of applicant's claimed "master management processor...configured to introduce marker information into the data to ensure that the integrity of the data is reasonably maintained when a link aggregation is modified" (as amended).

Applicant respectfully asserts that Figure 2 from Lee simply teaches fault handling logic 214, where "[f]ault handling logic 214 responds to fault indications" (Paragraph 0028 - emphasis added). However, disclosing fault handling logic for responding to fault indications fails to even suggest "[a] master management processor...configured to introduce marker information into the data to ensure that the integrity of the data is reasonably maintained when a link aggregation is modified" (emphasis added), as claimed by applicant.

Additionally, with respect to Claim 9, the Examiner has relied on item 214 of Figure 2 from Lee to make a prior art showing of applicant's claimed "selectively introducing marker information into the data to ensure that the integrity of the data is reasonably maintained when a link aggregation is modified" (as amended).

As noted above, applicant respectfully asserts that item 214 of Figure 2 from Lee simply discloses fault handling logic 214, where "[f]ault handling logic 214 responds to fault indications" (Paragraph 0028 - emphasis added). However, disclosing fault handling logic for responding to fault indications fails to even suggest "selectively introducing marker information into the data to ensure that the integrity of the data is reasonably maintained when a link aggregation is modified" (emphasis added), as claimed by applicant.

Again, since foregoing anticipation criterion has simply not been met by the above reference, as noted above, a notice of allowance or specific prior art showing of

each of the foregoing claim elements, in combination with the remaining claimed features, is respectfully requested.

Still yet, applicant brings to the Examiner's attention the subject matter of new Claims 10-12 below, which are added for full consideration:

"wherein the statistics are based on port traffic" (see Claim 10);

"further comprising sending a marker to facilitate handover from a first port to a second port" (see Claim 11); and

"wherein local ports on the switch are aggregated" (see Claim 12).

Again, a notice of allowance or a proper prior art showing of all of applicant's claim limitations, in combination with the remaining claim elements, is respectfully requested.

Thus, all of the independent claims are deemed allowable. Moreover, the remaining dependent claims are further deemed allowable, in view of their dependence on such independent claims.

In the event a telephone conversation would expedite the prosecution of this application, the Examiner may reach the undersigned at (408) 505-5100. The

Commissioner is authorized to charge any additional fees or credit any overpayment to Deposit Account No. 50-1351 (Order No. RMI1P013).

Respectfully submitted,
Zilka-Kotab, PC

/KEVINZILKA/

Kevin J. Zilka
Registration No. 41,429

P.O. Box 721120
San Jose, CA 95172-1120
408-505-5100